Journal of Information Hiding and Multimedia Signal Processing ©2018 ISSN 2073-4212
Ubiquitous International Volume **9**, Number **5**, September **2018**

Design of a Cyclic Self-Triggered DPWM for Resolution Extension

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Received January, 2018; revised May 2018

Abstract. *In many industrial applications such as motors, robots, and inverters, a digital pulse width modulation (DPWM) device is an important component. However, for extending its resolution, the conventional counter-based DPWM requires a higher reference clock frequency in proportion to its resolution bits. This paper proposes a DPWM device that uses a cyclic self-trigger of a monostable multivibrator to extend its resolution without increasing the reference clock frequency. Moreover, it maintains a low hardware complexity similar to the conventional counter-based DPWM.*
Keywords: Counter-based DPWM, Hardware complexity, Self-trigger, Resolution

1. **Introduction.** For achieving better power control in many control systems, pulse width modulation (PWM) is an important technology to control the average output voltage by adjusting its duty cycle [1]. The use of digitalized control can improve the cost and performance of a system; therefore, the digital PWM (DPWM) scheme is widely applied to motors, inverters [5,6], and DC-DC converters [7,8]. Increase in the resolution of a DPWM can result in precise output regulation and reduce unnecessary quantization error [3], however, a counter-based DPWM requires a reference clock frequency in proportion to its resolution, and thus, the increase in clock frequency may incur more dynamic power consumption and noise interference when a high resolution is set. For example, an 8-bit counter-based DPWM has a PWM pulse with an output frequency of 1 MHz, and it requires a reference clock frequency of up to 256 MHz. In this paper, a new DPWM device using a self-trigger based on a one-shot circuit is proposed to extend its resolution. The proposed DPWM does not require a high clock frequency to achieve the same resolution as a conventional counter-based DPWM. Furthermore, it only adds a reasonable hardware complexity when extending the resolution as compared to the delay-line DPWM described in the next section.

2. **DPWM Schemes.** Nowadays there are two main types of DPWM, which are implemented by counter and delay-line, respectively. For less hardware complexity and clock frequency, even both are combined as a hybrid DPWM [4]. The following sub-sections will introduce these two basic DPWM schemes.

2.1. **Counter-Based DPWM.** The counter-based DPWM, which is the simplest digital PWM scheme, can be easily implemented using an n-bit counter, an n-bit digital comparator, and an SR flip-flop as shown in Fig. 1 [2], where the comparing value of the digital comparator can be set by the digital setting code K. Initially, the counter value is zero and the output (Q) of the SR flip-flop is "Lo". Each positive transit of the reference clock will make the counter counts, which is similar to the ramp generation behavior of an analog PWM. Once the OV signal indicating the increment overflow of the counter appears, it will immediately turn the output of the SR flip-flop to "Hi". When the value of the counter equals to K, the output (A=B) of the comparator will reset the SR flip-flop, and it remains at the low state until the next overflow occurs. Therefore, a modulated pulse width corresponding to K will be generated from the output of the SR flip-flop. In fact, the SR flip-flop also can be removed, and the PWM output can still be achieved directly from the other output (A<B) of the comparator. For a given PWM output frequency f_{PWM}, an n-bit counter-based DPWM requires a reference clock frequency of $f_{CLK} = 2^n \times f_{PWM}$, thus, the duty cycle D of the counter-based DPWM is given as follows [9]:

$$D = \frac{T_K}{T_{PWM}} = \frac{K \times T_{CLK}}{2^n \times T_{CLK}} = \frac{K}{2^n} \tag{1}$$

where T_K represents the ON duration of the PWM pulse and varies from 0 to $2^n - 1$ clocks by adjusting the K value. When the counter-based DPWM tries to extend its resolution, the frequency of the reference clock will significantly increase [9]. Therefore, this DPWM scheme is not suitable for implementations with high resolution.

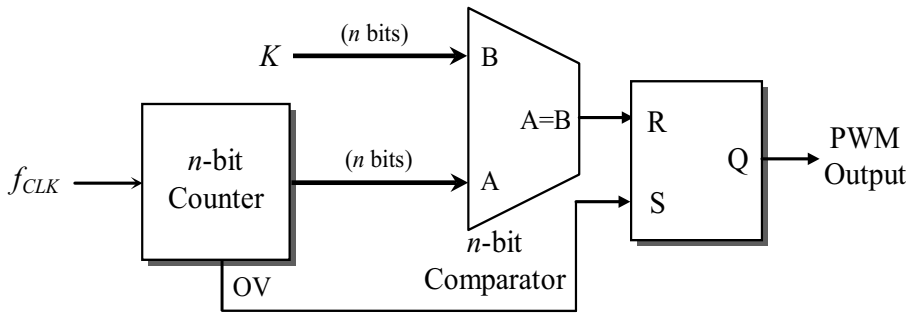


FIGURE 1. Basic structure of a counter-based DPWM

2.2. **Delay-Line DPWM.** An alternative DPWM scheme shown in Fig. 2, delay-line DPWM [3, 4], is one of the most commonly used approaches to avoid using a high-frequency clock that is required for the conventional counter-based DPWM. It consists of a cascade of delay cells, a large-scale multiplexer, and an SR flip-flop. Each delay cell produces a short delay time depending on the reference clock time and the number of delay cells. When the clock enters into the tapped delay line, the SR flip-flop is set to "Hi". By the selection of an n-bit setting code, the desired delay signal appears at the output of a 2^n to 1 multiplexer, and then the SR flip-flop is reset until the next clock enters the delay line again. Therefore, a modulated pulse width can be generated from the output of the SR flip-flop. Due to a mismatch in delay cells caused by process/temperature variations, the linearity of the delay-line DPWM may be affected. For better performance and linearity, the delay-line DPWM requires more number of hardware components, thus resulting in the device occupying a larger area [3, 4].

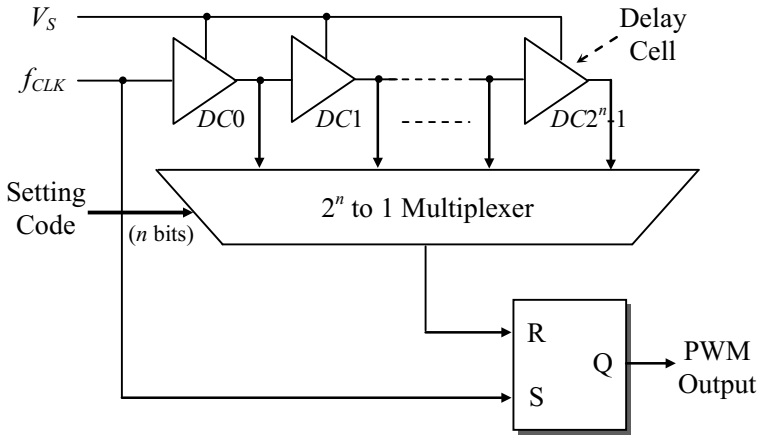


FIGURE 2. Basic structure of a delay-line DPWM

3. **Proposed DPWM Using a Self-Trigger.** For extending the resolution of the conventional counter-based DPWM, a new approach, namely a self-trigger based on a one-shot circuit, is used to increase the resolution of a DPWM without a high-frequency reference clock and much hardware complexity. The design details of the proposed DPWM are described in the following sub-sections.

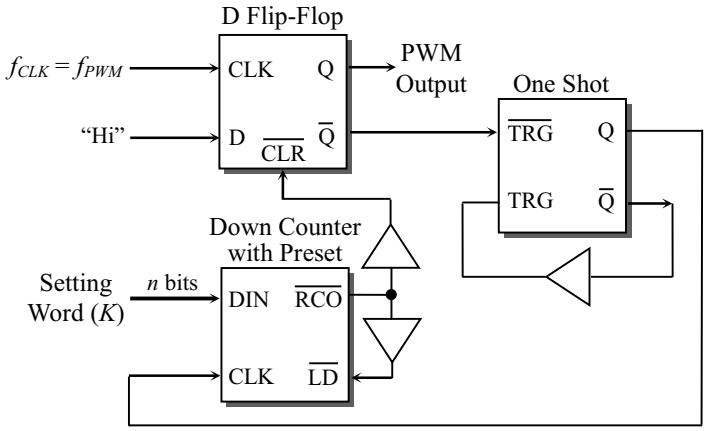


FIGURE 3. Architecture of the proposed DPWM

3.1. **Circuit Architecture.** The architecture of the proposed DPWM, shown in Fig. 3 [10], consists of a down counter with a preset, a monostable multivibrator (one shot) with positive-edge and negative-edge triggers, a D flip-flop, and some buffers. The setting code K can be automatically loaded into the down counter when it generates a ripple clock output each time. The clock to the down counter is generated by the one shot using the self-trigger method. The pulse width generated from the one shot depends on its external resistor and capacitor. In addition, several buffers are used to achieve the appropriate circuit delay time for avoiding unnecessary glitches.

3.2. **Principle and Operation.** At the initial state, the down counter presets its content by loading the setting code (K), and the output of the D flip-flop is set to "Lo". If K is set to zero, the ripple clock output (/RCO) of the down counter always clears the D flip-flop, and thus, no PWM output is produced. When the reference clock ($f_{CLK} = f_{PWM}$) enters into the D flip-flop at $K \neq 0$, its output becomes "Hi" immediately. Simultaneously, the

other complementary output will trigger the one shot to generate a pulse with time t_p connected to the clock input of the down counter, and the one shot feedbacks its other output (/Q) to the positive-edge trigger input. After a delay time (t_d) of the one shot, one pulse is generated again by itself; therefore, the one shot will commence continuous self-triggers as shown in Fig. 4 [10]. Meanwhile, the down counter counts down from the K value at each triggered pulse. When the down counter reaches zero, its /RCO output will clear the D flip-flop and re-load the K value into the counter, thereby the self-trigger operation of the one shot is stopped. During this period, the output of the D flip-flop remains at the "Lo" state until the next transition of the reference clock occurs. Therefore, via such a repeated operation, the PWM output modulated by K can be generated from the output of the D flip-flop without increasing the frequency of the reference clock.

According to the concept of an n-bit counter-based DPWM, the period time of the PWM output T_{PWM} is given by $2^n \times T_{CLK}$. If an n-bit resolution exists in one period time of the PWM for the proposed DPWM, the generated pulse width plus the component delay would be as follows:

$$t_p + t_d = T_{CLK} \tag{2}$$

Therefore, for a given PWM frequency and resolution, the pulse time t_p is found as:

$$t_p = \frac{T_{PWM}}{2^n} - t_d \tag{3}$$

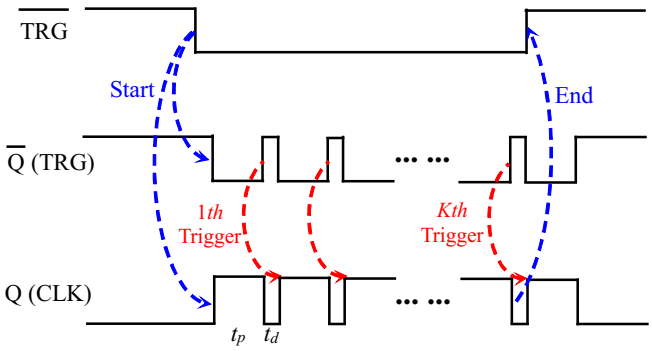


FIGURE 4. Self-trigger operation of one shot

3.3. **Benefits and Overheads.** By using a self-trigger of the one shot, the main contribution of the proposed DPWM scheme is to avoid using a high-frequency clock while seeking high resolution, therefore, the unnecessary power consumption and noise interference caused by high-frequency switching can be reduced. Compared with the frequently used delay-line DPWM, which has a large hardware requirement for satisfying high resolution and improving the linearity and performance of delay cells, the proposed DPWM has a lower hardware complexity, even with the addition of a one shot and several buffers.

Due to the use of an RC-based one shot in the proposed DPWM, capacitance error may affect precision of the duty cycle. Furthermore, the propagation delay of the one shot may limit the generated PWM frequency under an expected bit resolution, or may reduce its resolution for a given PWM frequency. However, this problem can be improved if an integrated circuit (IC) is used to replace discrete components in the implementation of the proposed DPWM.

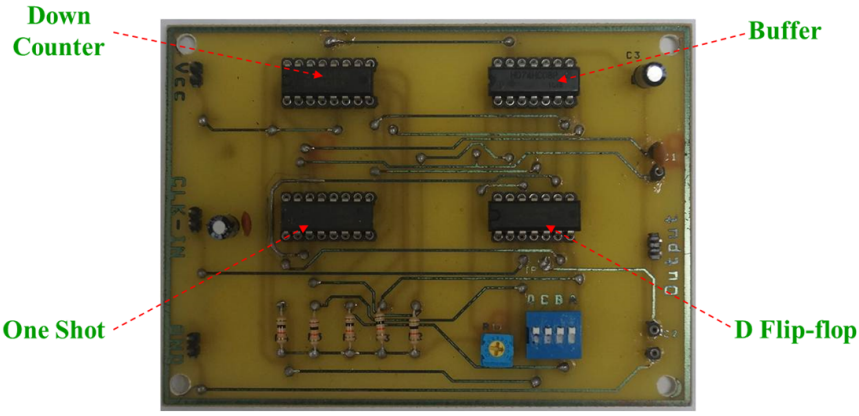
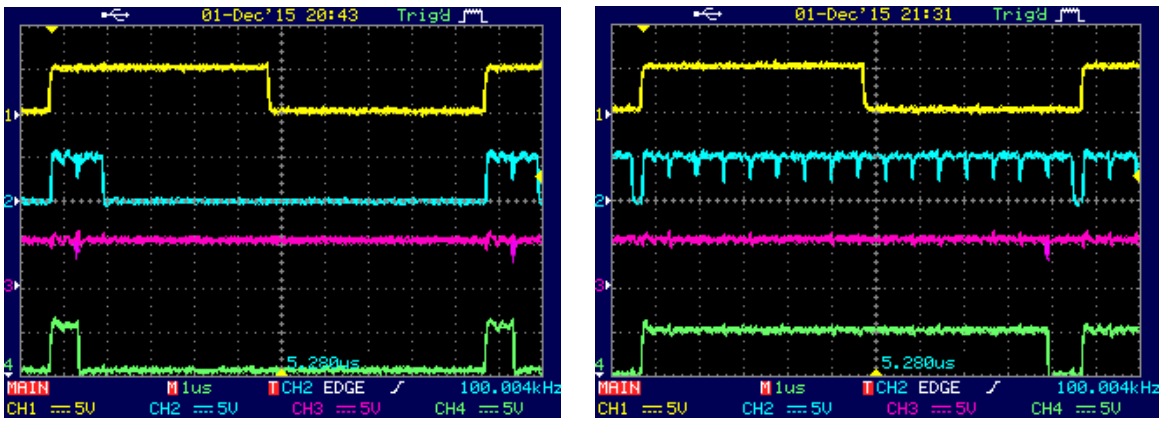


FIGURE 5. Circuit prototype of the proposed 4-bit DPWM

4. **Experimental Results.** To verify the operation of the proposed DPWM, we used discrete logical devices such as the 74HC191 (down counter), the 74HC74 (D flip-flop), and the 74HC123 (one shot) to construct a 4-bit DPWM, shown in Fig. 5. For a given PWM output of 100 KHz, the RC time constant of the one shot was selected to achieve a minimum pulse width of 625 ns for a 4-bit resolution according to Eq. 3. Furthermore, we attempted to adjust the value of K from 0 to 15 to obtain different duty cycle rates for our proposed DPWM and the conventional counter-based DPWM, where the reference clock frequency of the conventional counter-based DPWM must be increased to 1.6 MHz for a 4-bit resolution. Table 1 shows that the duty cycle rates of both DPWM schemes at the same K value were similar to the ideal values. Fig. 6(a) and 6(b) show the measured waves captured by the 4-CH storage oscilloscope for the proposed DPWM at $K = 1$ and at $K = 15$, respectively. In Fig. 6, the waves from top to bottom separately indicate: f_{CLK}, CLK, CLR, and PWM Output, and we find that the number of clocks (CLK) resulted from self-trigger and delivered to the down counter is decided by K, and the CLR signal from /RCO of the down counter will occur at the last clock.



(a) K=1 (b) K=15

FIGURE 6. Measured waveforms at K=1 and K=15

5. **Conclusions.** A new DPWM device using a self-trigger is proposed to extend the resolution of the original counter-based DPWM while maintaining the same clock frequency.

TABLE 1. Duty cycle rates at different K values

Type / K	Ideal DPWM	Counter-Based DPWM (f_{CLK} = 1.6 MHz)	Proposed DPWM (f_{CLK} = 100 KHz)
$K = 0$	0	0	0
$K = 1$	0.0625	0.0623	0.0631
$K = 2$	0.125	0.1249	0.1263
$K = 3$	0.1875	0.1876	0.1883
$K = 4$	0.25	0.2503	0.2511
$K = 5$	0.3125	0.3128	0.3127
$K = 6$	0.375	0.3754	0.3758
$K = 7$	0.4375	0.4382	0.4391
$K = 8$	0.5	0.5012	0.5011
$K = 9$	0.5625	0.5638	0.5628
$K = 10$	0.625	0.626	0.6257
$K = 11$	0.6875	0.6887	0.6889
$K = 12$	0.75	0.7497	0.7509
$K = 13$	0.8125	0.8134	0.8128
$K = 14$	0.875	0.8758	0.8757
$K = 15$	0.9375	0.9391	0.9378

According to practical experimental results, the proposed DPWM successfully generates a PWM output with a 4-bit resolution, and its duty cycle can be adjusted from 0% to 93.78%. Moreover, the proposed DPWM has a lower hardware complexity compared with the delay-line DPWM, and therefore is suitable for low-cost DPWM designs.

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