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FPGA Demonstration for WLAN-OFDM Baseband Receiver

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Abstract. *The FPGA demonstration for WLAN-OFDM baseband receiver is presented in this paper. In this OFDM baseband receiver, the CORDIC computing is employed to realize various arithmetics of baseband signal process and then to reduce the computational complexity of baseband receiver. For a large open office channel with 100 ns RMS delay spread, the measured EVMs of WLAN-OFDM baseband receiver are* -13.3, -16.6, -25.4 *and* -31.0 *dB for BPSK, QPSK, 16-QAM and 64-QAM, respectively. Finally, the physical design of WLAN-OFDM baseband receiver with 0.18 μm 1P6M CMOS technology indicates that the core area and power consumption are 1.2 mm*^{2} *(1094 μm* $\times$ *1092 μm) and 33.2 mW, respectively, with supply voltage of 1.8 V and operating clock of 40 MHz.*

Keywords: Coordinate Rotation DIgital Computer, Orthogonal Frequency Division Multiplexing , Field-Programmable Gate Array, Carrier Frequency Offset, Bit Error Rate, Signal-to-Noise Ratio, Error Vector Magnitude.

1. **Introduction.** For an orthogonal frequency-division multiplexing (OFDM) baseband transceiver, the primary operations of digital signal processing (DSP) include channel-estimation and -equalization, inverse fast-Fourier transformation (IFFT) and FFT, coarse- and fine-symbol boundary detection, coarse and fine carrier frequency offset (CFO) estimation, transmitting and receiving filter, etc. Actually, the vital computations for realizing these DSPs are constructed by multiplication, division, addition, subtraction, accumulation, look-up table (LUT) and so on.

The wireless local area network (WLAN) OFDM transceiver [1][2] is realized using joint algorithm [3] so that the OFDM receiver can not only obtain the accurate estimation and

compensation for CFO and channel distortion but also yield the lowest computational complexity compared with the considered algorithms [6] and [7]. On the other hand, the advantage of COordinate Rotation DIgital Computer (CORDIC) calculator can carry out various baseband computations, including multiplication, division, addition, subtraction, accumulation, arctangent, square-root, etc., based on the settings of *circular*- and *linear*-rotation with *rotation*- and *vectoring*-mode. Consequently, the CORDIC calculator can be employed to realize the essential computations of joint algorithm in WLAN-OFDM receiver and then to decrease the computational complexity of hardware implementation.

In this paper, the field-programmable gate array (FPGA) demonstration for WLAN-OFDM receiver is presented to realize the joint carrier synchronization and channel equalization algorithm [3] using CORDIC calculator. Totally, there are 3 CORDICs used in the WLAN-OFDM baseband receiver. The paper is organized as follows, the mathematical model of joint algorithm is briefly derived in Section 2. The CORDIC computing algorithm is firstly introduced in Section 3. Then, the hardware design of baseband receiver is also described based on CORDIC computing. The FPGA demonstration and the physical design are illustrated in Section 4. Finally, the conclusions are given in Section 5.

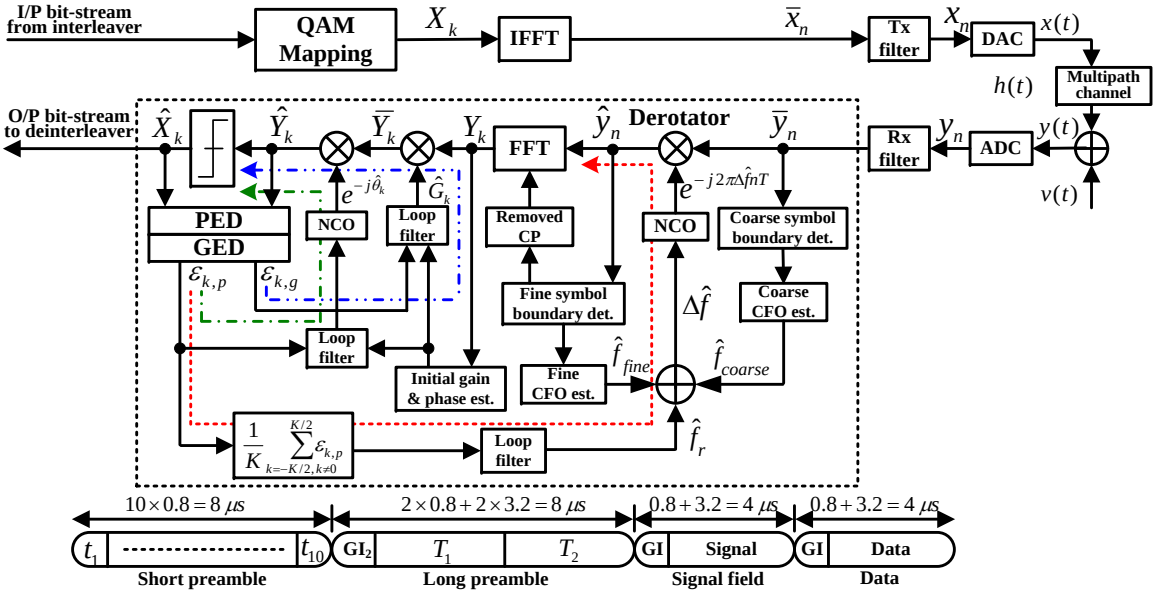


FIGURE 1. Block diagram of WLAN-OFDM transceiver (top) and the preamble structure (bottom).

2. **Mathematical Model of Joint Algorithm.** The block diagram of WLAN-OFDM transceiver is illustrated in the top of Fig. 1, where the receiver enclosed with dash-line is realized by joint algorithm [3]. As a matter of fact, the joint algorithm is constructed by a carrier synchronization and a channel equalization schemes, and briefly described in the following subsections.

2.1. **Carrier Synchronization Scheme.** The carrier synchronization is used to obtain the estimated CFO $\Delta\hat{f}$, as shown in Fig. 1, for compensating the CFO Δf. Actually, the estimated CFO is equivalent to the summation of $\hat{f}_{coarse}$, $\hat{f}_{fine}$ and $\hat{f}_r$. The $\hat{f}_{coarse}$ and the $\hat{f}_{fine}$ can be acquired by the coarse- and the fine-CFO estimations in the short- and the long-preamble duration as shown in the bottom of Fig. 1, respectively. In addition, the $\hat{f}_r$ is the estimated residual CFO and then employed to recover f_r, which is equal to Δf-$(\hat{f}_{coarse} + \hat{f}_{fine})$. Significantly, the carrier synchronization scheme of joint algorithm is composed of a frequency- and a phase-tracking loops with the red dash- and the green dash-dot-line, respectively, as illustrated in Fig. 1.

2.1.1. ***Frequency-Tracking Loop***. It is employed to acquire $\hat{f}_r$ for cancelling the phase offset in the time domain. In general, a derotator is used to perform the phase offset cancellation and the derotator output is expressed as

$$\hat{y}_{n,l} = e^{-j\hat{\phi}_n} \cdot (\hbar_n \otimes y_{n,l}) \tag{1}$$

where $\otimes$ is a convolution operator. $\hat{\phi}_n$ is equivalent to $2\pi\Delta\hat{f}nT$, where $\Delta\hat{f} = \hat{f}_{coarse} + \hat{f}_{fine} + \hat{f}_r$. The $\hbar_n$ is the impulse response of receiving filter. The $y_{n,l}$ is the nth output sample of ADC in the lth OFDM symbol and equal to

$$y_{n,l} = \left[y\left(t\right) \cdot e^{j2\pi\Delta ft}\right]_{t=l(N+N_g)T+N_gT+nT} \tag{2}$$

where $y(t)$ is the channel output with the continuous time. Both N_g and N express the length of cyclic-prefix (CP) and the number of FFT points, respectively. T is a sample interval and equivalent to T_u/N, where T_u is the FFT duration. Actually, Eq. (1) can be viewed as a frequency subtraction, where the frequency error f_e is equal to $\Delta f - \Delta\hat{f}$. The frequency error is transferred to the frequency domain as the normalized CFO error $\epsilon_e = f_eNT$, that induces the phase rotation on each subcarrier. Consequently, the phase distortion caused by the normalized CFO error will be compensated by a phase-tracking loop constructed on each subchannel in the frequency domain.

2.1.2. ***Phase-Tracking Loop***. Considering the phase rotation on each subcarrier, the kth subchannel of the lth OFDM symbol at FFT output [3] is given as

$$Y_{k,l} \approx e^{j\pi\epsilon_e\frac{N-1}{N}} \cdot e^{j2\pi\epsilon_e\frac{lN_s+N_g}{N}} \cdot \mathbf{H}_{k,l} \cdot X_{k,l} + V_{k,l} \tag{3}$$

where X_k and V_k express the transmitted symbol and the additive white Gaussian noise, respectively, on the kth subchannel. The $\mathbf{H}_{k,l}$ is the kth subchannel response of the multipath frequency selective fading channel and equivalent to $G_{\mathbf{H}_{k,l}} \cdot e^{j\theta_{\mathbf{H}_{k,l}}}$, where $G_{\mathbf{H}_{k,l}}$ and $\theta_{\mathbf{H}_{k,l}}$ are the magnitude and the phase distortions, respectively. Therefore, Eq. (3) can be reformulated as

$$Y_{k,l} = G_{k,l} \cdot e^{j\theta_{k,l}} \cdot X_{k,l} + V_{k,l} \tag{4}$$

where G_k and θ_k are the magnitude and the phase distortions of the kth ***equivalent subchannel***, respectively.

The phase-tracking loop is constructed on each subchannel to recover the constellation rotation resulted from the phase distortion θ_k, which is composed of the normalized CFO error ϵ_e and the channel phase distortion $\theta_{\mathbf{H}_{k,l}}$ as described in Eq. (3) and (4).

2.2. **Channel Equalization Scheme.** The channel equalization scheme of joint algorithm is divided into two operations, such as the magnitude- and the phase-equalization, and built on each subchannel. Fortunately, the phase-equalization on each suchannel can be fulfilled by cooperating with the phase-tracking loop as described in Section 2.1.2. The magnitude-equalization is used to compensate the magnitude distortion of multipath frequency selective fading channel.

2.3. **Subchannel Output.** After the compensations of phase-tracking loop and magnitude-equalization, the subchannel output can be derived as

$$\hat{Y}_{k,l} = \hat{G}_{k,l} \cdot e^{-j\hat{\theta}_{k,l}} \cdot Y_{k,l} \tag{5}$$

where $\hat{G}_k$ and $\hat{\theta}_k$ are the estimated magnitude and phase obtained from the magnitude-equalization and the phase-tracking loop, respectively, to compensate the the magnitude- and phase-distortion on the kth subchannel.

3. The CORDIC Computing for Baseband Receiver.

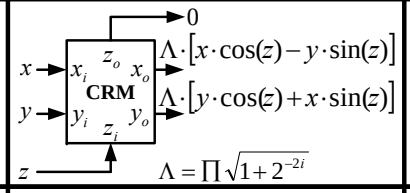
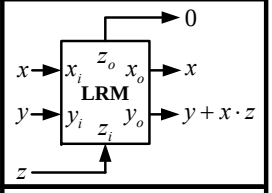
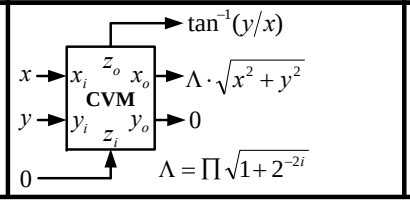
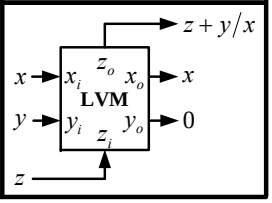
3.1. The Unified CORDIC Algorithm.

The unified CORDIC computing [4] is a robust arithmetic algorithm and has 3-type of rotation-mode including circular-, linear- and hyperbolic-rotation. In general, both the circular- and the linear-rotation are applied to the digital communication signal processing such as phase rotation, multiplication, division, square-root, arctangent, etc. The unified CORDIC algorithm is given as

$$\begin{aligned} x_{i+1} &= x_i - \lambda d_i y_i 2^{-i} \\ y_{i+1} &= y_i + d_i x_i 2^{-i} \\ z_{i+1} &= z_i - d_i \rho_i \end{aligned} \tag{6}$$

where i is the number of iterations for CORDIC computing. λ is a selection of rotation-type, ρ_i is a basic rotation angle of the ith iteration and d_i is a mode-selection for *rotation*- and *vectoring*-mode.

TABLE 1. The Parameter Setting of CORDIC Computing.

rotation / mode	Circular rotation		Linear rotation	
	$\lambda = 1$	$\rho_i = \tan^{-1}(2^{-i})$	$\lambda = 0$	$\rho_i = 2^{-i}$
Rotation mode $d_i = \mathrm{sgn}(z_i)$				
Vectoring mode $d_i = -\mathrm{sgn}(x_i \cdot y_i)$				

In this FPGA demonstration, both circular- and linear-rotation of CORDIC algorithm, including circular rotation/vectoring mode (CRM/CVM) and linear rotation/vectoring mode (LRM/LVM), are employed to realize OFDM baseband receiver. The related parameters with corresponding mode for CORDIC computing are illustrated in Table 1. The $sgn(\cdot)$ is defined as a sign-function, where $sgn(x) = +1$ for $x \geq 0$ and $sgn(x) = -1$ for $x < 0$. The Λ can be viewed as a scaling factor for the outputs of both circular rotation- and vectoring-mode, where Λ is equivalent to $\prod\sqrt{1+2^{2i}}$ and further converges to 1.6467 for $i \geq 7$. In order to obtain exactly outputs for both modes, the scale-down operation has to be realized at the outputs for both modes to compensate the scaling factor of 1.6467. Significantly, the scale-down factor is equal to $1/\Lambda \approx 0.60725$ [5], which can be reformulated as

$$1/\Lambda \approx 2^{-1}\cdot[(1+2^{-2})\cdot(1-2^{-5})\cdot(1+2^{-8})\cdot(1-2^{-10})] \tag{7}$$

Obviously, the scale-down operation can be easily fulfilled by shift-and-add operation without physical multiplier.

3.2. Hardware Design of OFDM Baseband Receiver.

3.2.1. ***Baseband Receiver using CORDIC Computing***. According to the requirements of signal processing as described in Section 2, the baseband receiver with CORDIC computing for FPGA demonstration is illustrated in Fig. 2, where the CORDIC computing is employed to realize the derotator, the phase-compensation and the magnitude-equalization on each subchannel, the coarse- and fine-CFO acquisition, and the initial

magnitude- and phase-estimation. Actually, there are 3 CORDICs that are implemented in the baseband receiver. The first one is a CRM computing that is used to realize *derotator* in the time domain. The second one is a combo CORDIC that can be configured as CRM- or CVM-computing to perform the phase-compensation, the coarse- and fine-CFO acquisition, and the initial magnitude- and phase-estimation. The third one is also a combo CORDIC that can be set as LRM- or LVM-computing to fulfill the magnitude-equalization and the initial magnitude-estimation. The detail designs of three CORDICs are discussed in subsequent subsections.

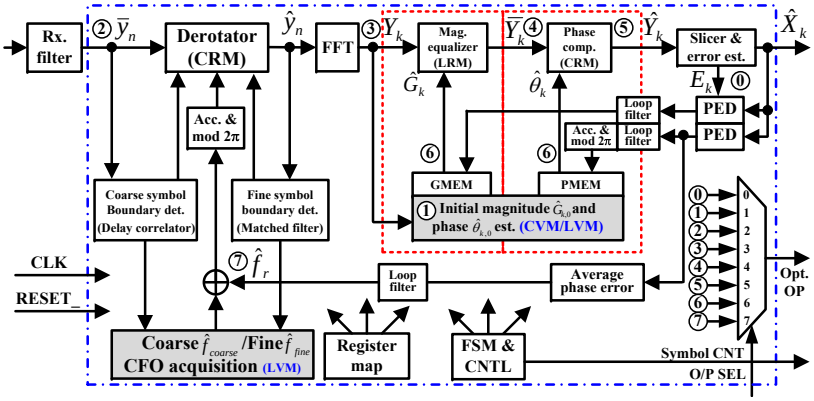


FIGURE 2. Baseband Architecture with CORDIC Computing for FPGA Demonstration.

3.2.2. ***CRM Computing for Derotator***. The mathematical model of derotator is derived in Eq. (1) for removing the phase offset, induced by CFO, in the time domain. The architectures for traditional- and CRM-computing-derotator with a numerically controlled oscillator (NCO) are illustrated in Fig. 3 (a). In order to reduce the hardware complexity, the traditional derotator and the sin/cos look-up-table (LUT), enclosed with dash-dot-dot line, can be replaced by the CRM computing derotator.

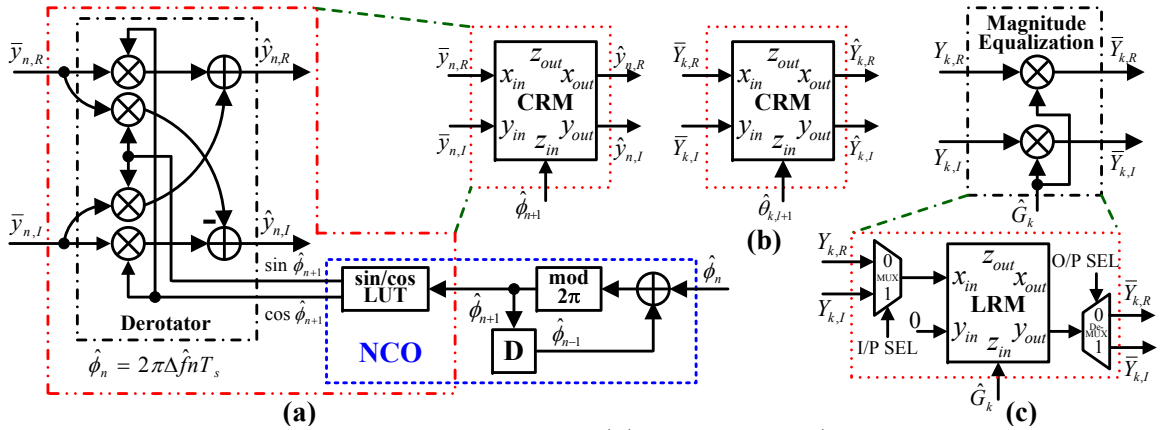
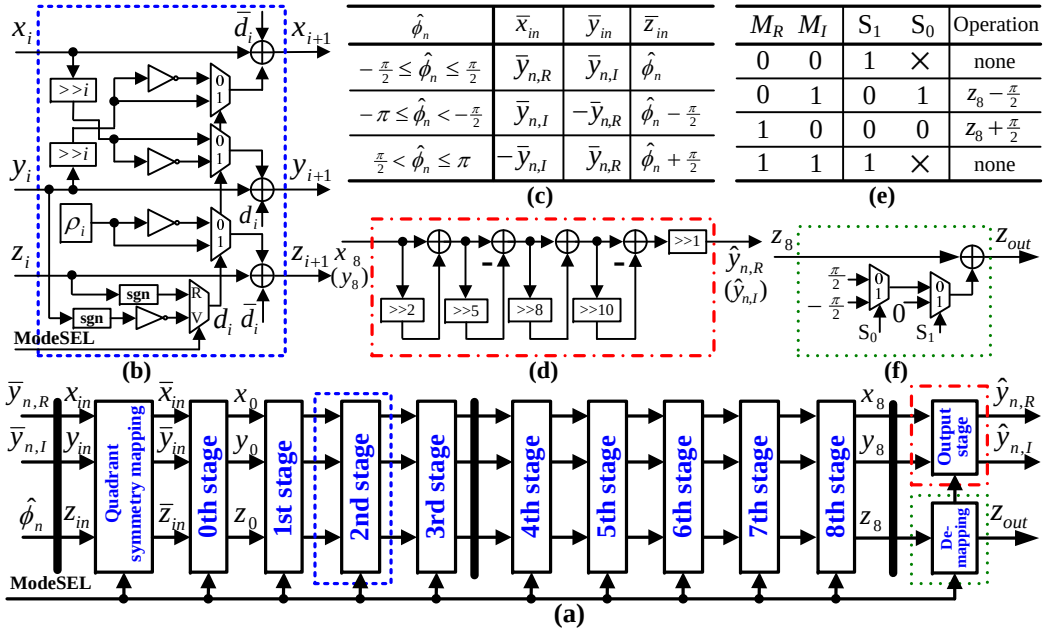


FIGURE 3. Derotator architecture for (a) traditional- (enclosed with dash-dot line) with NCO (surrounded with dash line) and CRM-computing-approach (encircled with dot line), and (b) phase-compensation architecture for CRM-computing-approach on each subchannel, and (c) magnitude-equalization architecture for traditional- (enclosed with dash-dot line) and LRM-computing-approach (encircled with dot line).

The CRM computing derotator has 9-stage and its circuit architecture is illustrated in Fig. 4 (a) excluding **demapping** and **ModeSEL**, where the 3 vertical bold lines express the pipelined stage. The circuit architecture of CORDIC cell for each stage, neglecting

the related parts of **ModeSEL**, is shown in Fig. 4 (b). Due to the rotation angle of CRM computing is limited by the range of $[-99.9^\circ\ 99.9^\circ]$, x_{in}, y_{in} and z_{in} are performed by the **quadrant symmetry mapping**, while $z_{in} > 90^\circ$ or $z_{in} < -90^\circ$. The operation of quadrant mapping is shown in Fig. 4 (c). The circuit architecture of output stage, as depicted in Eq. (7), is illustrated in Fig. 4 (d).



$\hat{\phi}_n$	$\bar{x}_{in}$	$\bar{y}_{in}$	$\bar{z}_{in}$
$-\frac{\pi}{2} \le \hat{\phi}_n \le \frac{\pi}{2}$	$\bar{y}_{n,R}$	$\bar{y}_{n,I}$	$\hat{\phi}_n$
$-\pi \le \hat{\phi}_n < -\frac{\pi}{2}$	$\bar{y}_{n,I}$	$-\bar{y}_{n,R}$	$\hat{\phi}_n - \frac{\pi}{2}$
$\frac{\pi}{2} < \hat{\phi}_n \le \pi$	$-\bar{y}_{n,I}$	$\bar{y}_{n,R}$	$\hat{\phi}_n + \frac{\pi}{2}$

M_R	M_I	S_1	S_0	Operation
0	0	1	×	none
0	1	0	1	$z_8 - \frac{\pi}{2}$
1	0	0	0	$z_8 + \frac{\pi}{2}$
1	1	1	×	none

FIGURE 4. (a) Circuit architecture for combo CRM/CVM CORDIC, (b) CORDIC cell, (c) the operation of quadrant mapping, (d) the circuit architecture of output stage, and (e) the truth table and (f) the circuit architecture of demapping.

3.2.3. ***Combo CRM/CVM CORDIC***. The circuit architecture of combo CRM/CVM CORDIC is shown in Fig. 4 (a). Actually, the combo CRM/CVM CORDIC is primarily used to realize the phase-compensation as depicted in Fig. 3 (b).

1. **Phase-Compensation**: The phase-compensation is constructed on each subchannel in the signal- and data-filed reception for recovering the constellation rotation resulted from the normalized CFO error ϵ_e and the channel phase distortion $\theta_{\mathbf{H}_k}$. The mode selection (**ModeSEL**) should be set as "0" to perform CRM-computing for phase-compensation.
2. **Coarse- and Fine-CFO Acquisition**: In the short- and long-preamble reception as shown in the bottom of Fig. 1, the combo CRM/CVM CORDIC with setting **ModeSEL**="1" can be configured as CVM-computing to fulfill the coarse- and fine-CFO acquisition. According to the ML algorithm [8], the coarse- and file-CFO estimation can be obtained as

$$\hat{f}_{coarse} = -\frac{1}{2\pi L_{16} T_{16}} \cdot \angle C_{16} \quad \text{and} \quad \hat{f}_{fine} = -\frac{1}{2\pi L_{64} T_{64}} \cdot \angle C_{64} \tag{8}$$

where L_{16} (T_{16}) and L_{64} (T_{64}) express the lengthes (periods) of short- and long-preamble, respectively. Both C_{16} and C_{64} represent the moving-sum outputs of delay correlator for short- and long-preamble, individually. The delay-correlator outputs of short- and long-preamble are equivalent to $\sum_{n=0}^{L_{16}-1} \bar{y}_n \cdot \bar{y}^*_{n-L_{16}}$ and $\sum_{n=0}^{L_{64}-1} \hat{y}_n \cdot \hat{y}^*_{n-L_{64}}$, respectively. The $\angle(\cdot)$ can be obtained at the z_{out} of CVM-computing. Significantly, the demapping, located at the output of z_8, is used to do the inversion of quadrant

mapping since the inputs, x_{in} and y_{in}, are processed by the quadrant symmetry mapping. The truth table and the circuit architecture of demapping are shown in Fig. 4 (e) and (f), respectively, where M_R and M_I express the MSBs of x_{in} and y_{in}, respectively, S_1 and S_0 are the selection of multiplexer, and the "×" denotes the don't care term. The related circuit architecture for coarse- and fine-CFO acquisition, including the delay-correlator, the matched filter and the moving-sum, is shown in Fig. 5.

3. **Initial Magnitude- and Phase-Estimation**: The combo CRM/CVM CORDIC with setting **ModeSEL**="1" can be fitted as CVM-computing to accomplish the initial magnitude- and phase-estimation [3], which can be obtained as

$$\hat{G}_{k,0} = |X_k|/|Y_k| \quad \text{and} \quad \hat{\theta}_{k,0} = tan^{-1}(X_k Y_k^*) \tag{9}$$

where X_k and Y_k denote the transmitted and the received long preambles on the kth subchannel, respectively. The configured architecture of the initial magnitude- and phase-estimation with combo CORDIC computing is illustrated in Fig. 6, where **MMEM** and **PMEM** express the magnitude- and the phase-memory, respectively, to store the estimated magnitude- and phase-coefficient. Besides, **SEL** as shown in Fig. 6 is employed to select the input sources of combo CRM/CVM computing for realizing the initial magnitude- or phase-estimation. For a complex signal A, $|A| = \sqrt{\Re(A)^2 + \Im(A)^2}$ and $\angle(A) = \tan^{-1}[\Im(A)/\Re(A)]$. The detail operations for the initial magnitude- and phase-estimation are described as follows,

- For initial magnitude-estimation, it is composed of a $|\cdot|$ and a division operations that can be realized by CVM- and LVM-computing, respectively. The $|X_k| = 1$ since $X_k = 1$ or -1, $\forall\ k$ in long preamble period. Therefore, $\hat{G}_{k,0} = 1/|Y_k|$. First, the received Y_k is stored in **MMEM** as denoted with **M1** in Fig. 6. After completing the phase-estimation, the Y_k is read out from **MMEM** and fed into CRM/CVM to obtain $\sqrt{\Re(\cdot)^2 + \Im(\cdot)^2}$ as expressed with **M2**. Then, the $\sqrt{\Re(\cdot)^2 + \Im(\cdot)^2}$ is sent to LRM/LVM to acquire $\hat{G}_{k,0}$ as represented with **M3**. Finally, $\hat{G}_{k,0}$ is stored in **MMEM** as depicted with **M4**.
- For initial phase-estimation, it requires two operations such as $X_k Y_k^*$ and $tan^{-1}(\cdot)$. The $X_k Y_k^*$ as expressed with **P1** is realized by multiplier and inverter as enclosed with dash-dot-dot line in Fig. 6. In order to save hardware complexity, the 2's complement operation is replaced by 1's complement using inverter. After completing the $X_k Y_k^*$ operation, the result is fed into CRM/CVM to acquire $\hat{\theta}_{k,0}$. Eventually, $\hat{\theta}_{k,0}$ is stored in **PMEM** as depicted with **P2**.

3.2.4. ***Combo LRM/LVM CORDIC***. The circuit architectures of combo LRM/LVM CORDIC and its CORDIC cell are depicted in Fig. 7 (a) and (b), respectively. The combo LRM/LVM CORDIC is mainly employed to fulfill the magnitude-equalization as shown in Fig. 3 (c).

1. **Magnitude-Equalization**: The magnitude-equalization is also built on each subchannel to compensate the magnitude distortion G_k, as derived in Eq. (4), caused by the multipath frequency-selective fading channel in the signal- and data-field reception. In order to further reduce the hardware complexity, only one LRM-computing with multiplexer and demultiplexer is realized to perform the magnitude equalization.
2. **Initial Magnitude-Estimation**: The combo LRM/LVM CORDIC can be configured as LVM-computing that performs the reciprocal of $|Y_k|$.

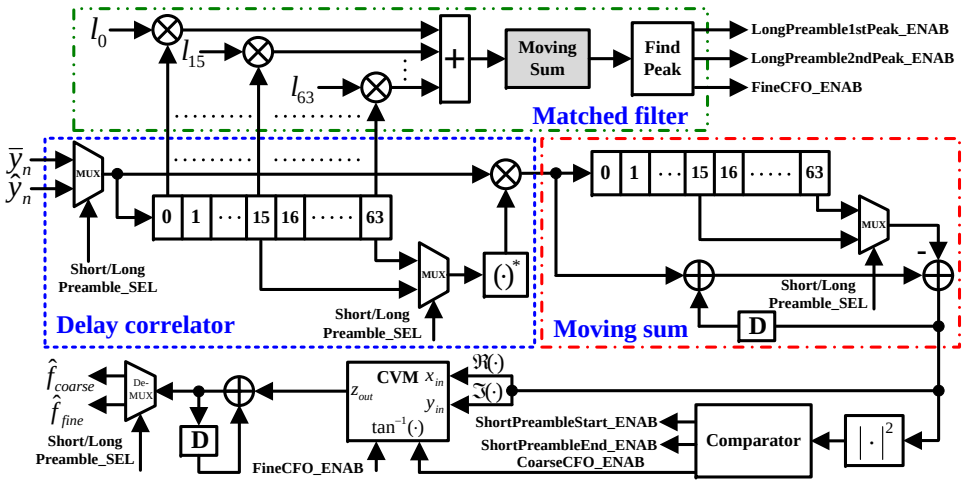


FIGURE 5. Circuit architecture for coarse- and fine-CFO acquisition, including the delay-correlator (coarse symbol boundary detection), the matched filter (fine symbol boundary detection) and the moving-sum.

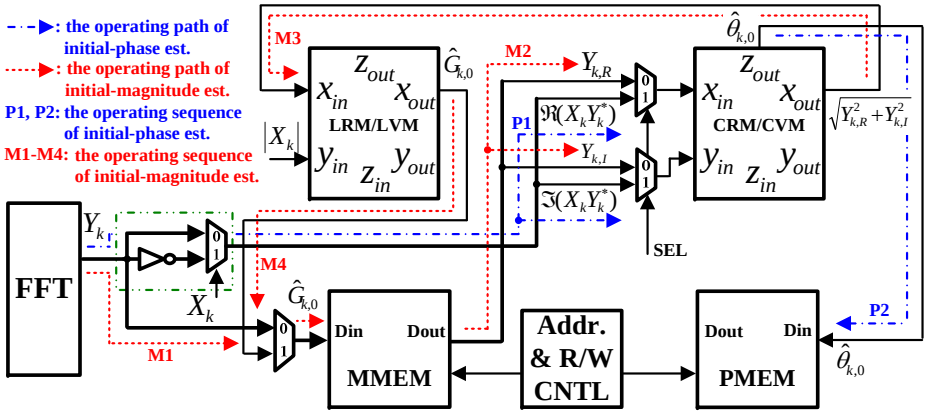


FIGURE 6. The configuration of initial magnitude- and phase-estimation.

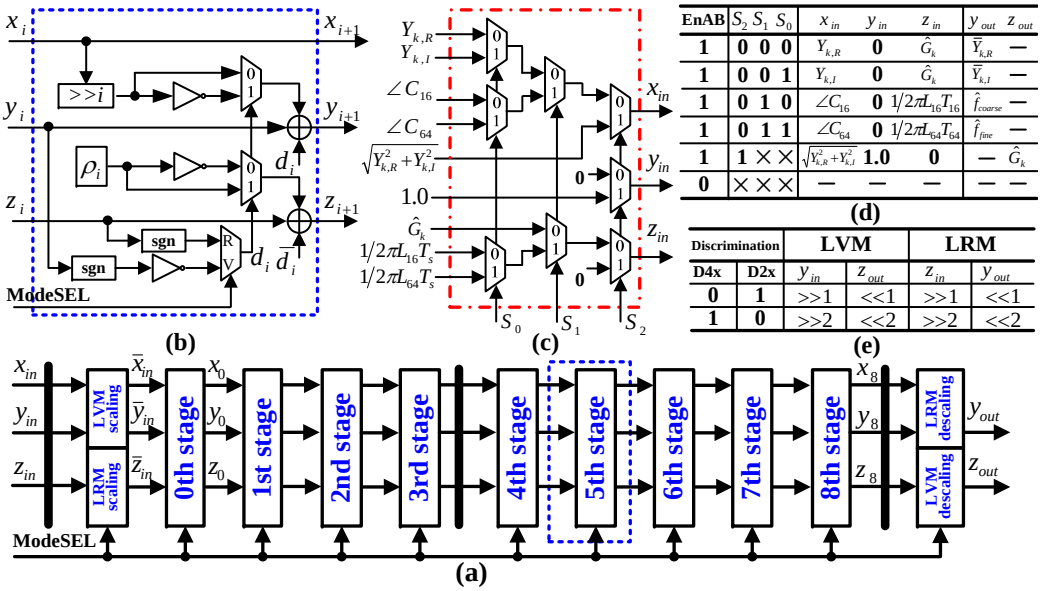
3. **Input-Selection- and Scaling-Module**: Due to various computations of combo LRM/LVM CORDIC, an input selection module, as depicted in Fig. 7 (c), is used to choose the input sources based on the different purposes, such as magnitude-equalization, initial magnitude-estimation, and coarse-/fine-CFO acquisition. The truth table of input selection module is shown in Fig. 7 (d). According to the limitations of multiplication (LRM) and division (LVM), the input and the output of combo LRM/LVM CORDIC have to perform scaling- and descaling-operation, respectively, and the related truth table is illustrated in Fig. 7 (e).

4. FPGA Demonstration and Physical Design.

4.1. FPGA Setup and Demonstration.

Both the floating- and the fixed-point *C* models are established to evaluate the OFDM transceiver as depicted in Fig. 1, where the related system parameters are listed in the left side of Table 2. The multipath frequency-selective fading channels, such as a typical office environment with 50 ns RMS delay spread (ChMA) and a large open space [9] with 100 ns RMS delay spread (ChMB), are built based on the statistical model [10].

For FPGA demonstration, the OFDM baseband receiver, enclosed with dash-dot line as shown in Fig. 2, is first realized by Verilog RTL, next synthesized by Quartus II, and then downloaded into FPGA development board (Stratix II EP2S180 F1020 C3)



EnAB	S_2 S_1 S_0	x_{in}	y_{in}	z_{in}	y_{out}	z_{out}
1	0 0 0	$Y_{k,R}$	0	$\hat{G}_k$	$\bar{Y}_{k,R}$	—
1	0 0 1	$Y_{k,I}$	0	$\hat{G}_k$	$\bar{Y}_{k,I}$	—
1	0 1 0	$\angle C_{16}$	0	$1/2\pi L_{16}T_{16}$	$\hat{f}_{coarse}$	—
1	0 1 1	$\angle C_{64}$	0	$1/2\pi L_{64}T_{64}$	$\hat{f}_{fine}$	—
1	1 × ×	$\sqrt{Y_{k,R}^2+Y_{k,I}^2}$	1.0	0	—	$\hat{G}_k$
0	× × ×	—	—	—	—	—

(d)

Discrimination		LVM		LRM	
D4x	D2x	y_{in}	z_{out}	z_{in}	y_{out}
0	1	>>1	<<1	>>1	<<1
1	0	>>2	<<2	>>2	<<2

(e)

FIGURE 7. (a) Circuit architecture for combo LRM/LVM CORDIC, (b) CORDIC cell, (c) the circuit architecture and (d) the truth table of input-selection-module, and (e) the truth table for input scaling and output descaling.

TABLE 2. The OFDM system parameter (left), the bit number of received signal path (middle) and the performance summary of physical design (right).

System parameter	IEEE 802.11a WLAN
Maximum CFO	±40 ppm (±232.2 KHz)
Sampling frequency (f_s)	40 (MHz)
Signal BW (f_B)	20 (MHz)
IDFT/DFT point	64
Data (N_d)/pilot (N_p) subcarrier	48/4
Subcarrier spacing (f_Δ)	312.5 (KHz)
IDFT/DFT (T) duration	3.2 (μs)
Symbol (N_s)/CP (N_g) length	80/16 (sample)
Symbol (T_s)/CP (T_g) duration	4.0/0.8 (μs)

Signal I/O	Bit no.
ADC	9
Rx filter O/P	12
Derotator O/P	13
Derotator phase I/P	11
FFT O/P	15
Init. mag. estimation	10
Init. phase estimation	12
Mag. equalization O/P	12
Phase comp. O/P	12

Modulation (uncoded data rate, Mbps)	WLAN-OFDM BPSK (12), QPSK (24), 16-QAM (48), and 64-QAM (72)
Process	0.18 μm 1P6M CMOS technology
Supply voltage (V)	1.8(core)/3.3(pad)
Operating clock (MHz)	40
Power Consumption (mW)	51/33.2 (core)
Area (mm^2)	1464×1462/ 1094×1092(core)
Normalized gate count	51,720

with power supply of 3.3 V and operating clock of 40 MHz as illustrated in Fig. 8 (a), where the measured equipment is Keysight 16823A Logic Analyzer (LA). Besides, the real-time measurements, including error vector magnitude (EVM), signal-to-noise ratio (SNR), constellation and eye-diagram, are displayed by using the vector signal analysis (VSA) on Keysight 16823A. The measured results for BPSK, QPSK, 16- and 64-QAM with the maximum CFO (±232.2 KHz) over ChMB are depicted in Table 3. The measured EVMs for BPSK, QPSK, 16- and 64-QAM are -13.3, -16.6, -25.4 and -31.0 dB, respectively, and meet the required EVMs [11]. In addition, the measured SNRs for QPSK, 16- and 64-QAM are 16.9, 22.8 and 27.3 dB, respectively. Considering the symbol error rate (SER) measurement, the total number of measured subchannel symbols is larger than 5×10^4, which is approximately 1046 OFDM symbols. The SERs for 16- and 64-QAM over ChMA and ChMB are measured at FPGA output and illustrated in Fig. 9. Significantly, for given SNR≈26 dB and SER≈10^{-4} with 64-QAM as shown in Fig. 9, the system SNR degradation between the floating-point simulation and the FPGA measurement (or the

fixed-point simulation) is less than 0.3 dB, which is close to the design target of SNR loss (≤ 0.25 dB) [12] induced by hardware implementation.

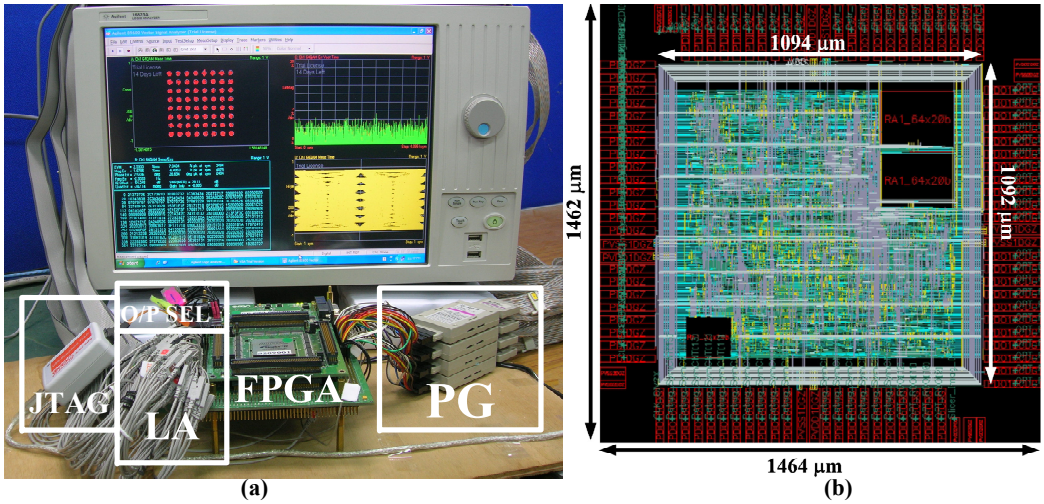
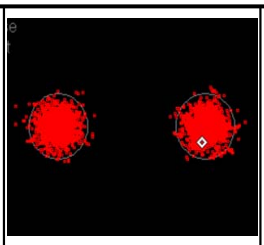
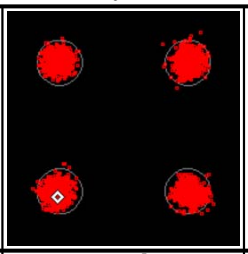
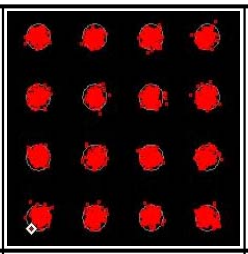
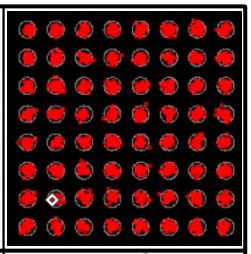


FIGURE 8. (a) FPGA demonstration and (b) physical layout.

TABLE 3. Performance Summary of FPGA Demonstration over ChMB.

Measured constellation					
EVM	**Measured**	**-13.3 dB**	**-16.6 dB**	**-25.4 dB**	**-31.0 dB**
	Required	**< -5 dB**	**-10 dB**	**-16 dB**	**< -25 dB**
Measured SNR		**--**	**16.9 dB**	**22.8 dB**	**27.3 dB**

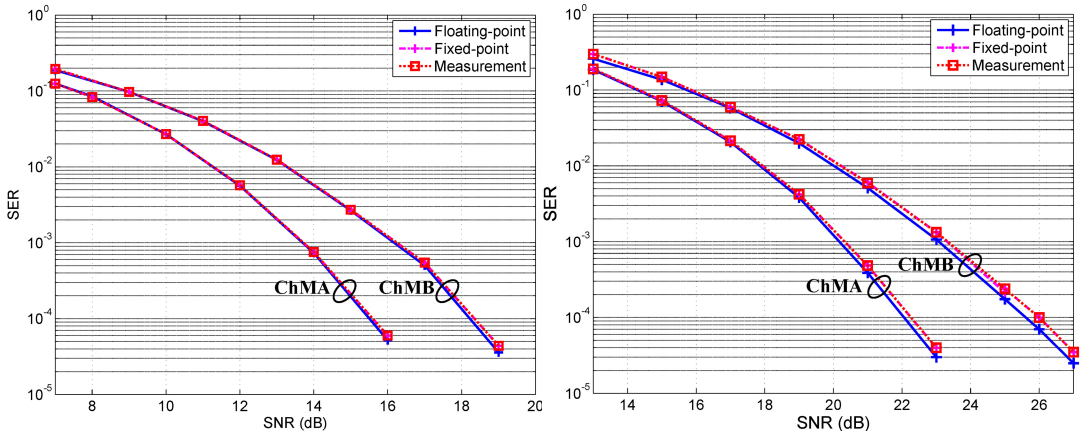


FIGURE 9. SERs of 16-QAM (left) and 64-QAM (right) over ChMA and ChMB.

4.2. **Physical Design and Discussion.** The physical design of baseband receiver is implemented by 0.18 μm 1P6M CMOS process and its layout is shown in Fig. 8 (b). The performance summary of physical design is illustrated in the right side of Table 2. The power consumption of baseband receiver, estimated by PrimeTime, is 51.0 mW with the supply voltages of 3.3 V (pad) and 1.8 V (core), and the operating clock of 40 MHz,

where the core power consumption is 33.2 mW. The chip area of baseband receiver is 2.1 mm^2 (1464 μm×1462 μm), where the core area is 1.2 mm^2 (1094 μm×1092 μm) and its normalized gate count is equivalent to 51,720.

TABLE 4. Comparison in hardware complexity, conventional approach vs. CRM computing for derotator implementation (top), and direct implementation vs. CORDIC computing with LRM/LVM and CRM/CVM for the magnitude-equalization, the phase-compensation and the initial magnitude/phase estimation (bottom).

Derotator	Two π/4 ROMs (256×11b) for sin/cos LUT (mm^2)			Complex mult. (mm^2)	Total (mm^2)	Reduction efficiency
Traditional approach	sin	cos	combinational logic	4-mult & 2-add	0.123	57.7%
	0.04	0.04	0.003	0.040		
CRM computing	0.052					

Direct implementation	Mag. eq.	Initial mag. est.			Init. ph. est.	Phase compensation		Total (mm^2)	Reduction efficiency
	× *	$\Re(\cdot)^2+\Im(\cdot)^2$	$\sqrt{(\cdot)}$	÷	$\tan(\cdot)^{-1}$	4-mult & 2-add	2 π/4 ROMs & comb. logic		
	0.013	0.004 #	0.004	0.022	0.006	0.045	0.083	0.177	46.8%
Combo LRM/LVM	0.032							0.094	
Combo CRM/CVM	0.062								

*: Only a multiplier employed to realize the magnitude-equalization and to obtain $\Re(\cdot)^2$ and $\Im(\cdot)^2$.
#: Just an adder used to fulfill the addition for $\Re(\cdot)^2$ and $\Im(\cdot)^2$.

In order to evaluate the cost-effective design of CORDIC-computing, the comparisons in hardware complexity are illustrated in Table 4. Considering the discussion for traditional- and CRM-computing-derotator as described in Section 3.2.2, the circuit architecture of sin/cos LUT, used for NCO, is composed of a $\frac{\pi}{4}$ sin ROM, a $\frac{\pi}{4}$ cos ROM and some combinational logics, and shown in Fig. 10. Both ROMs, generated by Artisan memory compiler, are the same size. For traditional-detroator, the rest of components, including multiplier, adder and combinational logic, are called from DesignWare library. The reduction efficiency of hardware complexity of CRM-computing derotator can reach 57.7% compared with that of traditional approach.

Regarding the combo CRM/CVM and LRM/LVM CORDICs, we only consider the direct implementation for realizing the magnitude-equalization, the phase-comparison, and the initial magnitude- and phase-estimation. In order to do a fair comparison, only a multiplier is used to fulfill the magnitude-equalization and also to obtain $\Re(\cdot)^2$ and $\Im(\cdot)^2$. Hence, $\Re(\cdot)^2+\Im(\cdot)^2$ is just realized by an adder. The circuit architecture of phase-compensation can be viewed as the same as that of traditional detorator. Consequently, the reduction efficiency of hardware complexity of combo CRM/CVM and LRM/LVM CORDICs can achieve 46.8% compared with that of direct implementation.

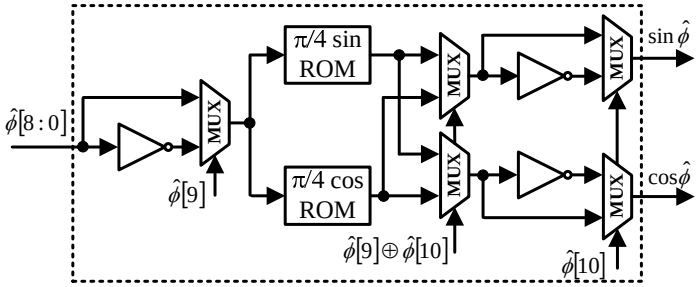


FIGURE 10. Circuit architecture of sin/cos LUT for NCO implementation.

5. **Conclusions.** In this paper, the total of 3 CORDICs is employed to realize the related baseband signal processes of WLAN-OFDM baseband receiver including the derotator, the magnitude-equalization, the phase-compensation, and the initial magnitude- and phase-estimation, etc. The FPGA demonstration for this WLAN-OFDM baseband receiver is also presented to on-line measure EVMs and SNRs. Significantly, the measured EVMs of WLAN-OFDM baseband receiver for a large open office with 100 ns RMS delay spread are −13.3, −16.6, −25.4 and −31.0 dB for BPSK, QPSK, 16- and 64-QAM, respectively. The physical design of WLAN-OFDM baseband reciver is realized with 0.18 μm 1P6M CMOS process. The chip area is 2.1 mm^2 (1464 μm $\times$ 1462 μm), where the core area is 1.2 mm^2 (1094 μm $\times$ 1092 μm). The chip power consumption with supply voltages of 1.8 V (core) and 3.3 V (pad), and operating clock of 40 MHz is 51.0 mW, where the core power consumption is 33.2 mW. Besides, for the realization of CRM-computing derotator, the reduction efficiency of hardware complexity can reach 57.7% compared with the traditional approach. Considering the implementation of magnitude-equalization, the phase-comparison, and the initial magnitude- and phase-estimation, using both combo CRM/LVM and LRM/LVM CORDICs approach can yield 47.7% reduction efficiency of hardware complexity compared with the direct implementation.

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